The application has been carefully reviewed in light of the Office Action dated September 17, 2003. Claims 1-20 are pending in this case.

Claims 1-4, 6, 8-14 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakajima et al. (U.S. Patent No. 6,181,314 B1) in view of Negishi et al. (U.S. Patent No. 5,528,241) and further in view of Yamagata et al. (U.S. Patent Application Publication No. US# 2001/0028336 A1). Applicants respectfully request reconsideration.

None of the references show "impedance converters connected to an output of a ladder resistor, gray level voltage wires constituting output lines connected to the impedance converters." Likewise, none of the references teach or suggest "gray level voltage wire[s] [each] connected to the output of the ladder resistor via impedance converters." The Office Action makes no contention to the contrary. The limitations quoted above are important aspects of the claimed inventions. Since none of the references show the limitations quoted above, any combination of such references will not meet the limitations either.

As explained in the previous response, Nakajima discloses a liquid crystal display device having output buffers corresponding to column lines, and comprising analog switches provided between output ends of the output buffers and the column lines respectively, and a switch controller for on-off controlling the analog switches. A DA converter is provided in the preceding stage of the output buffers, and the switch controller turns off the analog switches during a DA conversion period of the DA converter or during a precharge period prior to DA conversion, and turns on the analog switches during a predetermined period other than such periods.

In Fig. 2 of Nakajima, n output buffers 16 are connected between output circuit 17 and capacitance loads C1 to Cn through analog switches 18-1 to 18-n, which creates a problem since building in as many analog circuits as signal lines pulls down the yield of the display unit. (see specification page 1, lines 11-13). Claim 1 includes a drive unit

comprising a ladder resistor, impedance converters connected to an output of a ladder resistor, gray level voltage wires constituting output lines connected to the impedance converters, and a gray level voltage selector connected to the gray level voltage wires.

Negishi discloses a digital-to-analog converter having a ladder resistor portion for generating a plurality of quantization signals of predetermined values based on reference signals of predetermined values and a quantization switch portion for selectively outputting one of the quantization signals in accordance with a digital input value. The digital to analog converter disclosed in Negishi is merely a converter that includes a ladder-resistor type which includes serially connected 256 resistors R1...R256 of the same resistance value. A switch portion selectively connects junction points of the resistors to an input terminal of an amplifier to a second reference voltage.

Yamagata discloses gradation wiring for a display, a driver for a liquid crystal display and a stress test method which can detect insulation failure between the gradation wiring. Yamagata also discloses gradation wiring for a display, a driver for a liquid crystal display and a stress test method which can detect the insulation failure between the gradation wiring in a short period.

The integrated circuit disclosed in Yamagata includes an impedance converter, a ladder resistor, and gradation levels with six N-channel MOS transistors (transfer gates) Tr that are connected to respective negative gradation voltage lines NLN in series. The N-channel MOS transistors Tr are arranged as a two-dimensional matrix of 6 rows.times.64 columns. A signal line 3 from the negative data latch LT1 (FIG. 1) is connected to the gates of each transistor Tr. Depending upon a digital image data supplied to the signal line 3, one of sixty-four negative gradation voltage lines NLN is selected to output an analog gradation voltage to the negative operational amplifier OP1 (FIG. 1) via the signal line 4.

As illustrated in the attached sketch showing the devices of Nakajima, Negishi and Yamagata, the cited references merely teach a plurality of sets of an impedance

converter and a DA converter which fails to address the problems addressed by the present invention.

Dependent claims 5 and 7 should be allowable along with claim 1 and for other reasons.

Claims 15-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakajima, Negishi and Yamagata in view of Kane (U.S. Patent No. 6,229,508 B1). Applicants respectfully request reconsideration. As mentioned above with respect to claim 1, Nakajima, Negishi and Yamagata whether considered alone or in combination, fail to teach or suggest an image display apparatus comprising *inter alia* "impedance converters connected to an output of a ladder resistor, gray level voltage wires constituting output lines connected to the impedance converters." In addition, Kane fails to teach or suggest such an apparatus.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By _____

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